GRIDNET - Powerline Communication

1.2 APPLICATIONS OF PLC

- Home Automation
- Automatic Meter Reading
- Process Control
- Heating and Ventilation Control
- Air Conditioning Control
- Lighting Control
- Status Monitoring and Control
- Low Speed Data Communication Networks
- Intelligent Buildings
- Signs and Information Displays
- Fire and Security Alarm System
- Power Distribution Management

1.3 CHALLENGES OF PLC

Power lines and their associated networks are not designed for communication use. They are hostile environments that make the accurate propagation of communication signals difficult. Two of the biggest problems faced in using power lines for communications are excessive noise levels and cable attenuation. Noise levels are often excessive, and cable attenuation at the frequencies of interest is often very large. The most common causes of excessive noise in a domestic situation are the various household devices and office equipment connected to the network. Noise and disturbances on the power network include over voltages, under voltages, frequency variations and so on. However, the most harmful noise for PLC applications is that superimposed on a power line. Switching devices such as light dimmers, induction motors in many common appliances and high-frequency noise caused by computer monitors and televisions often causes such superimposed noise.

In this paper we present a simple hardware implementation for a PLC system using a microcontroller, which provides data generation and interfacing for the status and monitoring control for medical purposes. The system is suitable for other data communications within a local power network area, such as remote automatic meter reading, fire and security alarm control, etc. The system is built using on-off-keying (OOK) modulation to reduce complexity. The PLC system is connected to power lines using proper interfacing circuits which are used to provide electrical isolation and impedance adaptation between the microcontroller and the power line network. This means that the system can be implemented using the available off-the-shelf components and hence a great reduction in the cost of the overall system. The system was tested during many hours of continuous operation, and it was found that the transmitted signal suffered from small distortion levels.

Chapter 2
BACKGROUND

Communication techniques are seem to be viable to natural and cultural interferences like climatic conditions and cultural variations. How much we could eliminate the possible interruptions and disturbances of probabilistic nature, the better is the effectivity and convenience of different methods. There exists various conditions across India as well as around the globe where expertise doctors are seldom met. Especially among the tribal populations who are being getting neglected by changing governments and economic policies.

Tribals are a social group residing in definite area away from civilization and have cultural homogeneity and unifying social organization. India is home to 84.33 million people classified as tribals in our total population. There are 461 groups of tribes who are spread over 26 states and Union Territories with majority (87%) found in central belt of the country. Included in these categories are 74 tribes who have been identified as Primitive Tribal Groups (PTG, now called Particularly Vulnerable Group) characterized by pre-agricultural levels of technology, extremely low level of literacy and extreme poverty. In general, they live in isolated, scattered and difficult to reach terrain generally near hills and shrinking forests on which they depend for their livelihood. Majority of tribal literacy is meager and exist below poverty line making the economic, education and nutritional status worse compared to the generalpopulation.

In most tribal communities, medical care, treatment and etiology of disease are defined within the social context. It is important to identify processes by which tribals recognize sickness and the ways to counteract it. The illness could well be attributed to the evil eye, magic or offending some deity, the treatment for which could be through folk medicine or magico-religious methods. Religious rites are used mainly to treat diseases like small pox and propitiating the deity concerned, most of which tribals believe can cure the plagues, which are associated with various diseases. No comprehensive strategy has been formulated to deal with tribal health problems, as there is not enough knowledge available on their customs, beliefs and practices, which are intimately connected with the treatment of disease.

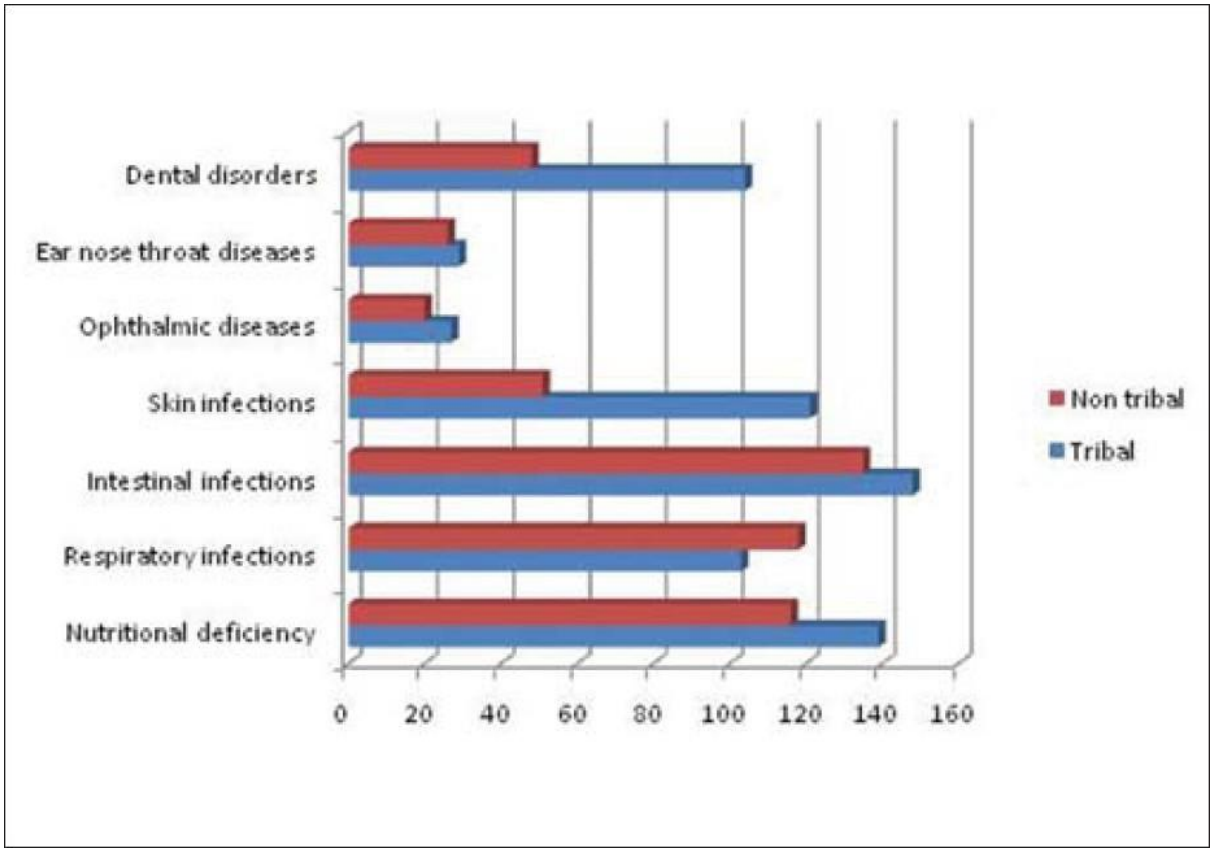


Fig 2.1 Comparison of infection rate between tribal and non-tribal population. Coutesy: MGO

Indicators	Situation in Maharashtra	Tribal Situation
Infant mortality rate	59	110
Crude death rate	7.9	13
Maternal mortality rate	2	Not available
LBW babies	28%	40%
Family Size	3.8	4.2
Delivery by TBA	86%	12%

Table 1: Health Status Indicators in Tribes
Courtesy:AIMS Study across Maharashtra

Proper medical assistances cannot me assured to them, since the doctors cannot promise 24 hour dedicated service due to transportation, cultural variations and other problems. Though the tribal people or the health warden in that area can communicate with the doctor through wireless medias , their given details may not be sufficient for the doctor to take proper decisions. If the doctors can monitor the status of the patients in accurate numerical terms continuously from any place ,then this could be a better alternative. The doctors can evaluate blood-pressure, body temperature, heartbeat, and other physical status of the patients through the sensors coupled to their body and hence they can suggest proper medicines to them.

We came to know about the uncompleted project namely 'Lady Health warden' which was put forward by the government of Pakistan for advancements in medical field among rural people and tribal populations. This was the first effort to provide primary health care to the vast rural population of Pakistan which was made in 1959, when the rural health program was launched to provide preventive and curative services by establishing 150 rural health centres. However the project succeed in providing only one RHC, with the three sub-health centres, to look after a population of 50,000.Primary Health Care project ,which replace the basic health services project, was initiated by the government of Pakistan and United States Agency For International Development (USAID)in September 1982. It was originally a 5 year project, but has since been extended to 1990. USAID supports this effort through its sponsorship of the 30 million dollar Primary Health Care Project, the goal of which is to expand and improve the quality of rural health services. They tried to utilize the 3 phase power-line which is available at all the health centres to communicate with the efficient doctors in any part of the country so that the health wardens can use the doctor's prescriptions and give proper treatment to the patients who are admitted in the health centres. The assignment of health warden was to provide a first-aid kit to each admitted patient and hence help the doctors in monitoring them. Unfortunately, the project couldn't meet the target effectively.

Chapter 4
IMPLEMENTATION

4.1 MICROCONTROLLER

The 8-bit microcontroller AT89C51 or AT89C52 from ATMEL is selected to control the system. This is a 40-pin chip, which contains four input /output ports, 256 bit ram, 8Kbyte of prom. The power is applied across the Vcc (pin 40) and GND (pin 20) pins. The external execution is eliminated by connecting the EA pin to Vcc through a resistor.

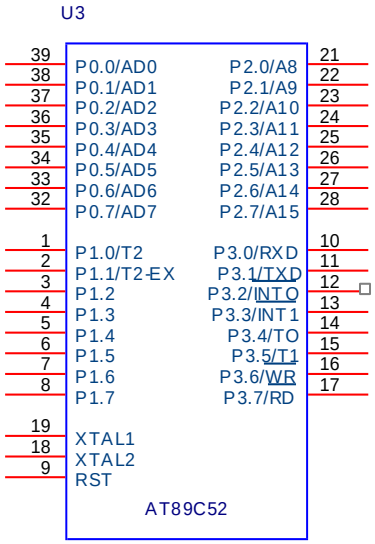


Fig4.1 Pinout dgm of AT89C52

The AT89C52 is a low-power, high-performance CMOS 8-bit microcomputer with 8K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high density non-volatile memory technology and is compatible with the industry standard 80C51 and 80C52 instruction set and pin out. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional non-volatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C52 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications. The AT89C52 provides the following standard features: 8K bytes of Flash, 256 bytes of RAM, 32 I/O lines, three 16-bit timer/counters, six-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89C52 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power down Mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next hardware reset.

4.1.1 PORT 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high impedance inputs. Port 0 can also be configured to be the multiplexed low order

address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

4.1.2 PORT 1

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. In addition, P1.0 and P1.1 can be configured to be the timer/counter 2 external count input (P1.0/T2) and the timer/counter 2 trigger input (P1.1/T2EX), respectively, as shown in the following table. Port 1 also receives the low-order address bytes during Flash programming and verification.

4.1.3 PORT 2

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that uses 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that uses 8-bit addresses (MOVX @ RI); Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

4.1.4 PORT 3

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pull-ups. Port 3 also serves the functions of various special features of the AT89C51, as shown in the following table. Port 3 also receives some control signals for Flash programming and verification.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

4.1.5 RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

4.1.6 ALE/PROG

Address Latch Enable is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

4.1.7 PSEN

Program Store Enable is the read strobe to external program memory. When the AT89C52 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

4.1.8 EA/VPP

'External Access Enable'. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions. This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming when 12-volt programming is selected.

4.1.9 CLOCK INPUTS

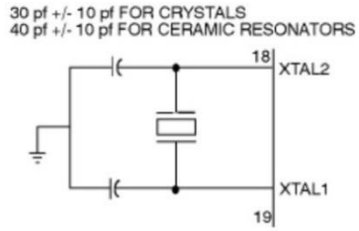


Fig4.2 Clock outputs

The X1 and X2 inputs are connected to the ends of a piezo electric crystal. We can choose the crystal frequency from 1Mhz to 24Mhz. Also both of the crystal inputs are connected to ground through capacitors of vale 33pf. The clock pin connection is shown below.

4.1.10 RESET INPUTS

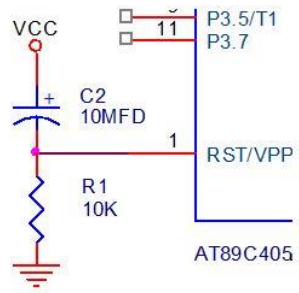


Fig4.3 Reset inputs

The figure shows the connections of the reset pin. The reset pin is connected to a power on reset circuit. The capacitor voltage at the time of power on will be 1. This will reset microcontroller. The voltage drops to zero shortly after some time. This will remove the reset condition and the microcontroller will start fetching now.

4.2 CARRIER WAVE GENERATOR

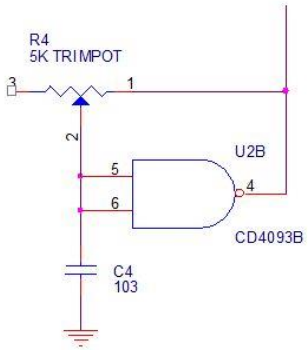


fig4.4 Carrier wave generator

An astable multivibrator is used generate the carrier frequency. In our case we are selecting a high frequency wave, frequency above 100hz, as the carrier wave. The carrier frequency is generated with the help of a NAND-Gate, which is wired as a NOT-gate. Further we will refer this gate a NOT-gate in this section.

The input voltage of the NOT gate will be at logic low level as soon as the power is switched ON, since the capacitor voltage is zero. This logic low-level input will make the output voltage at logic high level. Thus the capacitor charges to logic high level through the resistor. After some time, the capacitor voltage reaches the logic high level. This in turn makes the output of the NOT-gate as logic zero. Now the capacitor starts discharging through the resistor. The output level of the NOT-gate will remain at logic low level until the capacitor voltage discharges up to zero. The NOT-gate output will goes to logic high level as soon as the capacitor voltage is at logic low level and the capacitor starts charging. This process cycles infinitely.

4.3 MODULATOR AND POWER LINE INTERFACE

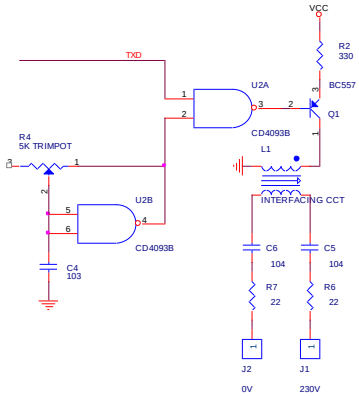


Fig4.5 Modulator And Power Line Interface

The carrier wave is applied to the Pin2 of the gate N2A. the other pin of this gate is connected to the TXD pin of the microcontroller. Therefore the output of this gate remains at logic high level as far as this TXD pin remains a logic low level. The carrier frequency can reach the output only when the TXD pin is kept at high level.

The output of this gate is connected to the base of an amplifier transistor. The amplified signal is applied to a tuned frequency transformer which will allow a narrow band of frequency to pass through it. The transformer is so adjusted that we will get maximum amplitude of voltage at the output of the transformer.

This transformer also provides isolation for between the 230V line and the 5V low potential line. The resistors and capacitors connected in series with the input of the transformer will limit the current flowing through the transformer. We had selected the carrier frequency so high in order to limit the short circuit for the carrier frequency through other electrical loads that are designed to work with 50Hz frequency.

4.4 CARRIER RECEIVER

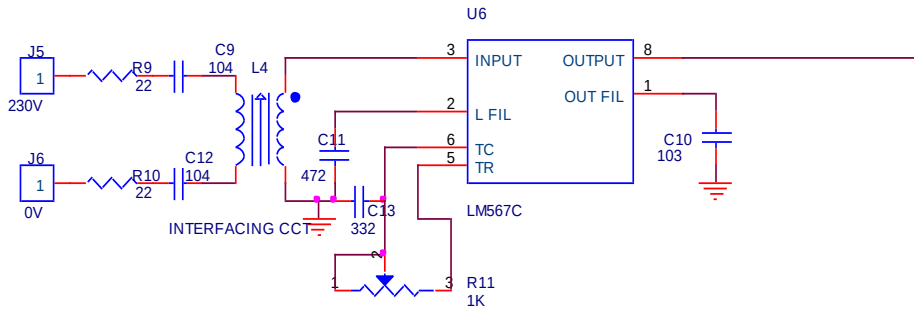


Fig4.6 Carrier Receiver

The receiver circuit is designed with the help of a Phase Locked Loop. The carrier frequency in the 230V line is by passed to the input of the Phase Locked Loop via a tuned frequency transformer. The series RC network at the input of this transformer adds high impedance to the low frequency 50Hz supply and steps up the high frequency wave.

The output of this transformer is connected to the input of the Phase Locked Loop IC that compares the input frequency with a reference frequency. In our project we are using LM567 / NE567 as the Phase Locked Loop. The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the pass band. The circuit consists of I and Q detector driven by a voltage controlled oscillator which determines the centre frequency of the decoder. External components are used to independently set centre frequency, bandwidth and output delay.

The centre frequency of the tone decoder is equal to the free running frequency of the VCO.

$$f_o \cong \frac{1}{1.1\ R_1\ C_1}$$

This is given by The bandwidth of the filter may be found from the approximation

$$BW = 1070 \sqrt{\frac{V_i}{f_o C_2}} \text{ in \% of } f_o$$

Where:

Vi = Input voltage (volts rms), Vi □ □200 mV

C2 = Capacitance at Pin 2 (μF)

The output of the Phase Locked Loop goes logic low level whenever the input frequency matches with the reference frequency. The output of the Phase Locked Loop is connected to the RxD pin of the UART in the microcontroller.

4.5 RELAY DRIVER AND RELAY

The relay is an electromagnetic device, which consists of solenoid, moving contacts, fixed contact and a restoring spring. The relay takes advantage of the fact that when electricity flows through a coil, it becomes an electromagnet. The electromagnetic coil attracts a steel plate, which is attached to a switch. So the switch's motion (ON and OFF) is controlled by the current flowing to the coil, or not, respectively.

A very useful feature of a relay is that it can be used to electrically isolate different parts of a circuit. It will allow a low voltage circuit (e.g. 5VDC) to switch the power in a high voltage circuit (e.g. 100 VAC or more). The relay operates mechanically, so it cannot operate at high speed.

Fig4.7 Relay driver and relay

There is much kind of relays. You can select one according to your needs. The various things to consider when selecting a relay are its size, voltage and current capacity of the contact points, drive voltage, impedance, number of contacts, resistance of the contacts, etc.

The resistance voltage of the contacts is the maximum voltage that can be conducted at the point of contact in the switch. When the maximum is exceeded, the contacts will spark and melt, sometimes fusing together. The relay will fail. The value is printed on the relay. Depending on the output connectivity the relays are classified into two.

Single pole double throw relay (SPDT)

Double pole double throw relay (DPDT)

The specification of the relay will contain the working voltage, solenoid impedance current and voltage rating of the contacts. Here we are using 12V, 100-ohm 6Amp Relays.

When we connect the rated voltage across the coil the back Emf opposes the current flow but after a short time the supply voltage will overcome the back emf and the current flow through the coil increase. When this current is equal to the activating current of the relay the core is magnetized and it attracts the moving contact. Now the moving contact leaves from its initial position where it makes a contact with a fixed terminal known as normally closed terminal (N/c).

Now the common contact or moving contact establishes a connection with a new terminal, which is indicated as normally open terminal (N/O). Whenever the supply to the coil is withdrawn the magnetizing force is vanished. Now the restoring spring pulls the moving contact back to initial position, where it makes a connection with N/C terminal. However it is also to be noted that at this time also a back Emf produced. The withdrawal time may be in microseconds, the back emf may be in the range of few kilovolts and in opposite polarity with the supply terminals. This voltage is known as surge voltage. It must be neutralized or else it may damage the system. A diode across the relay coil in reverse bias, will act as a short circuit for this surge voltage and it will neutralize here itself.

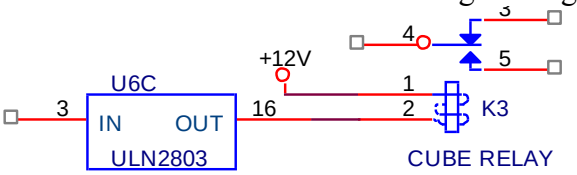


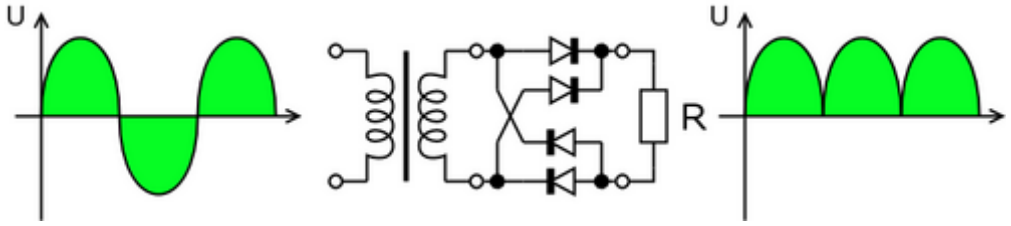
Fig4.8 ULN2803

In order meet the current and voltage requirement, we are using a dedicated relay driver IC ULN2803. The relay driver circuitry using this IC is very simple. The circuit is self explanatory.

4.6 POWER SUPPLY

The system requires a regulated +5v supply for the semiconductors and a +12V unregulated supply for the relay. These can be delivered from the 230V domestic supply. Before applying this to the system we must step down this high voltage to an appropriate value. After that it should be rectified. This will provide a unidirectional current. To achieve a +5V DC we should regulate this. All these are done in the power supply circuitry, which is explained below.

Full-wave rectification converts both polarities of the input waveform to DC, and is more efficient. However, in a circuit with a non-centre tapped transformer, four rectifiers are required instead of the one needed for half-wave rectification. This is due to each output polarity requiring two rectifiers each, for example, one for when AC terminal 'X' is positive and one for when AC terminal 'Y' is positive. The other DC output requires exactly the same, resulting in four individual junctions (See semiconductors/diode). Four rectifiers arranged this way are called a bridge rectifier:



A full wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output by reversing the negative (or positive) portions of the alternating current waveform. The positive (negative) portions thus combine with the reversed negative (positive) portions to produce an entirely positive (negative) voltage/current waveform

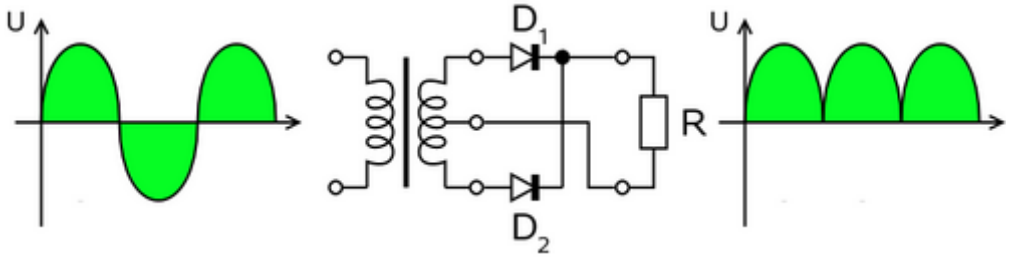


Fig4.9 Powersupply

4.6.1 RECTIFIER OUTPUT SMOOTHING

While half- and full-wave rectification suffices to deliver a form of DC output, neither produces constant voltage DC. In order to produce steady DC from a rectified AC supply, a smoothing circuit, sometimes called a filter, is required. In its simplest form this can be what is known as a reservoir capacitor, Filter capacitor or smoothing capacitor, placed at the DC output of the rectifier. There will still remain an amount of AC ripple voltage where the voltage is not completely smoothed.

Sizing of the capacitor represents a trade-off. For a given load, a larger capacitor will reduce ripple but will cost more and will create higher peak currents in the transformer secondary and in the supply feeding it. In extreme cases where many rectifiers are loaded onto a power distribution circuit, it may prove difficult for the power distribution authority to maintain a correctly shaped sinusoidal voltage curve.

For a given tolerable ripple the required capacitor size is proportional to the load current and inversely proportional to the supply frequency and the number of output peaks of the rectifier per input cycle. The load current and the supply frequency are generally outside the control of the designer of the rectifier system but the number of peaks per input cycle can be effected by the choice of rectifier design.

A half wave rectifier will only give one peak per cycle and for this and other reasons is only used in very small power supplies. A full wave rectifier achieves two peaks per cycle and this is the best that can be done with single phase input. For three phase inputs a three phase bridge will give six peaks per cycle and even higher numbers of peaks can be achieved by using transformer networks placed before the rectifier to convert to a higher phase order. To further reduce this ripple, a capacitor-input filter can be used. This complements the reservoir capacitor with a choke and a second filter capacitor, so that a steadier DC output can be obtained across the terminals of the filter capacitor. The choke presents high impedance to the ripple current. If the DC load is very demanding of a smooth supply voltage, a voltage regulator will be used either instead of or in addition to the capacitor-input filter, both to remove the last of the ripple and to deal with variations in supply and load characteristics.

4.7 THREE TERMINAL VOLTAGE REGULATOR

FOR ± 5V

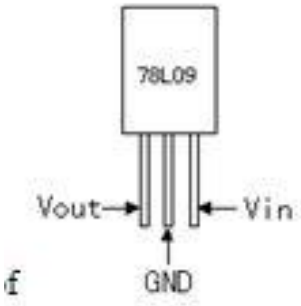


fig4.10 Three Terminal Voltage Regulator

The L7800 series of three-terminal positive regulators is available in TO-220 ISOWATT220 TO-3 and D2PAK packages and several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Three-terminal IC power regulators include on-chip overload protection against virtually any normal fault condition. Current limiting protects against short circuits fusing the aluminum interconnects on the chip. Safe-area protection decreases the available output current at high input voltages to insure that the internal power transistor operates within its safe area.

Finally, thermal overload protection turns off the regulator at chip temperatures of about 170°C, preventing destruction due to excessive heating. Even though the IC is fully protected against normal overloads, careful design must be used to insure reliable operation in the system.

4.7.1 FEATURES

1. Output current up to 1.5 A
2. Output voltages of 5; 4.2; 6; 8; 8.5; 9;12; 15; 18; 24V
3. Thermal overload protection
4. Short circuit protection
4. Output transition safe operating area protection

A 12-0-12V step down transformer is connected to provide the necessary low voltage. The transformer also works as an isolator between the hot and cold end. The hot end refers to the 230V supply, which is a hazardous one, and the cold one refers to the low, safe voltage. Now the hot portion appears only at the primary of the transformer. The secondary of the transformer deliver 12V ac pulses along with a ground.

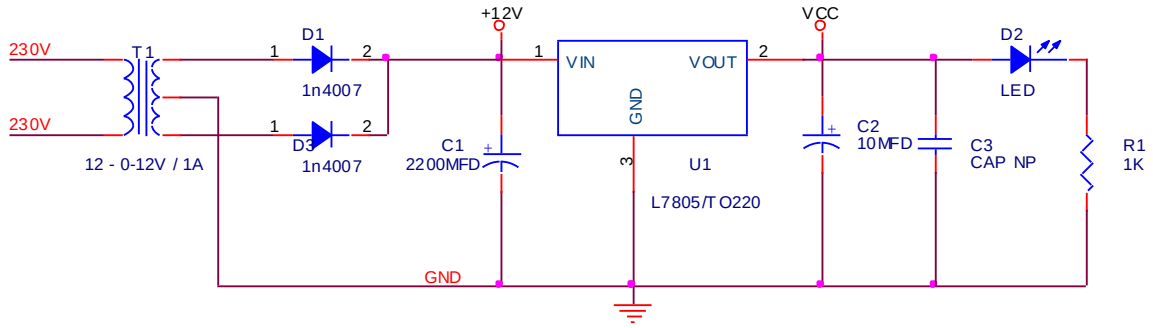


Fig 4.11 circuit diagram

This ac supply goes to a center tap rectifier, which converts the ac into a unidirectional voltage. The ripples in the resulting supply is filtered and smoothed by a 2200µFD/25V capacitor. The 0.1µF capacitor bypasses any high frequency noises. The resulting supply has the magnitude above 17V. This voltage is fed to the regulator IC 7804. This IC provides a regulated 5V positive supply at its 3rd pin. The required input for this is more than 7.5V. Also there is an LED in series with a 1K Ω resistor. This will act as a power ON indicator.

4.8 DUAL SUPPLY

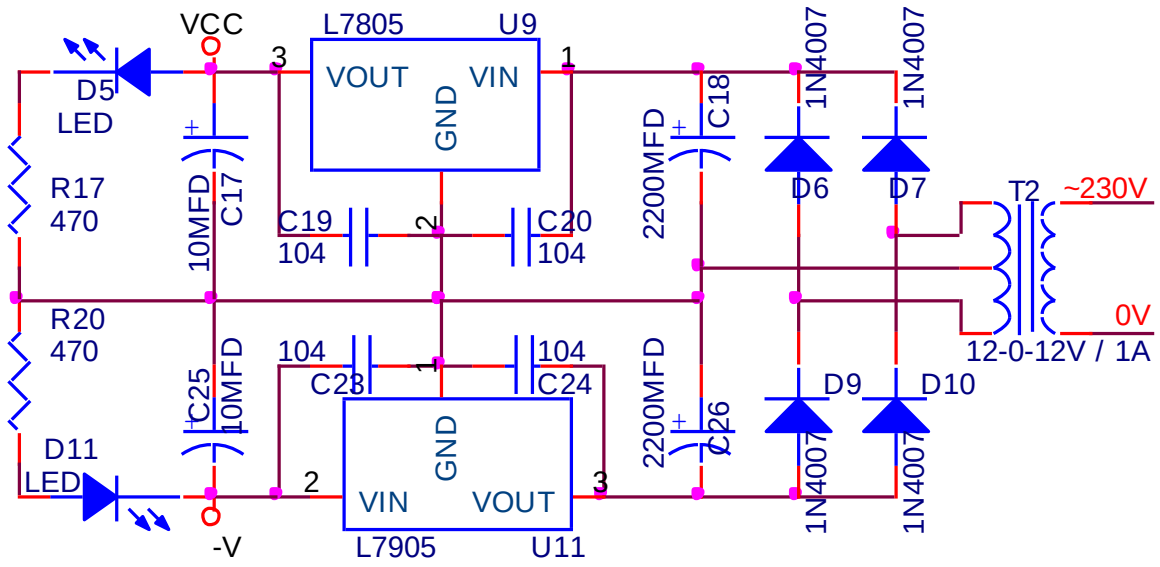


Fig4.12 Dual Supply

The unit requires a dual supply since operational amplifiers are employed in it. The dual supply can be obtained by utilizing center tapped bridge rectifier. The bridge rectifier provides +ve and –ve outputs with reference to the centre tap of the transformer. This can be filtered with capacitors and regulated with L7805 positive regulator and L7905 negative regulator. The LEDs provided at the output of the regulator IC s indicates power ON status.

Chapter 5
CIRCUIT DIAGRAM

5.1 TRANSMITTER SECTION

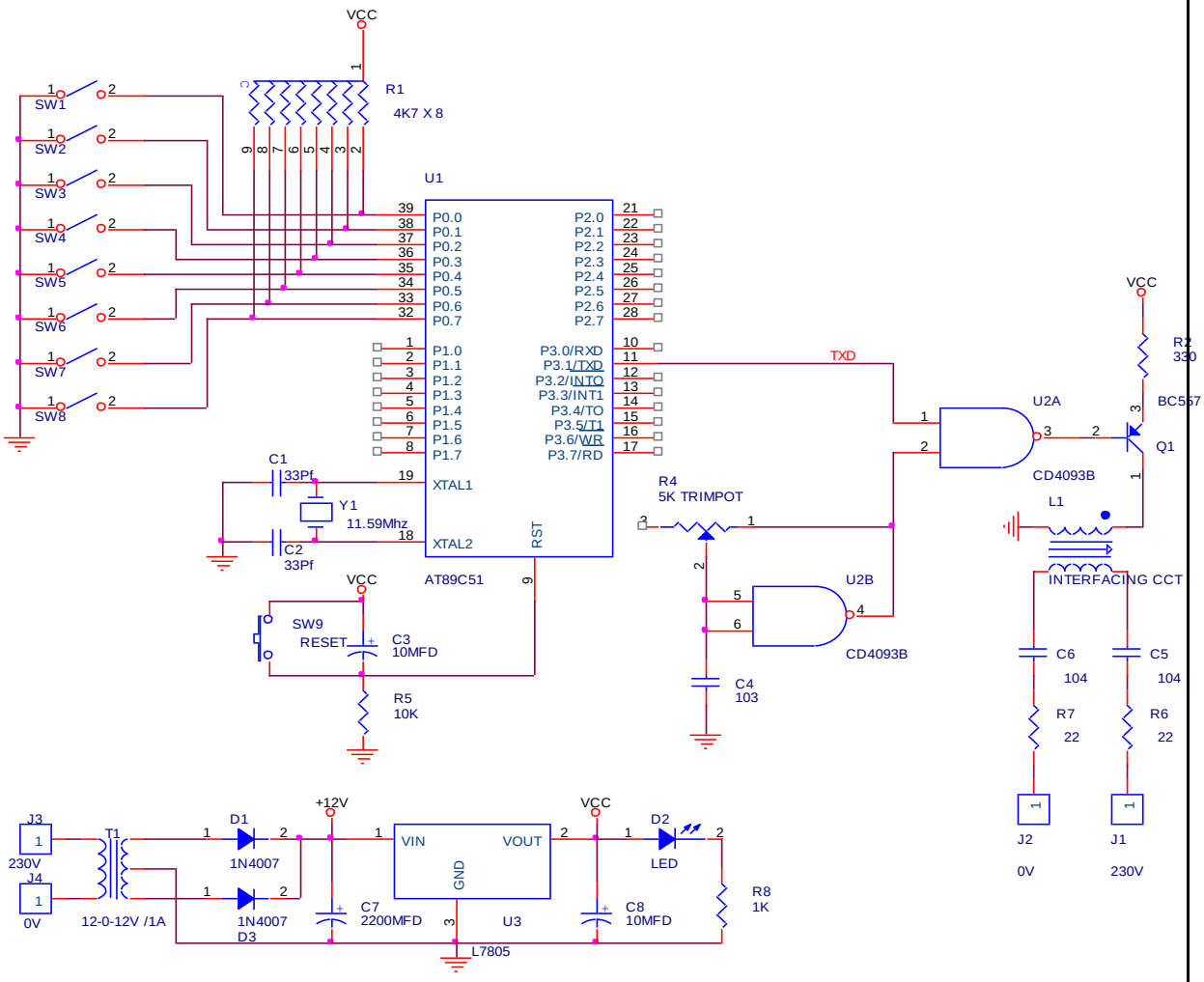


Fig5.1 Circuit diagram of Transmission Section

5.2 RECEIVER SECTION

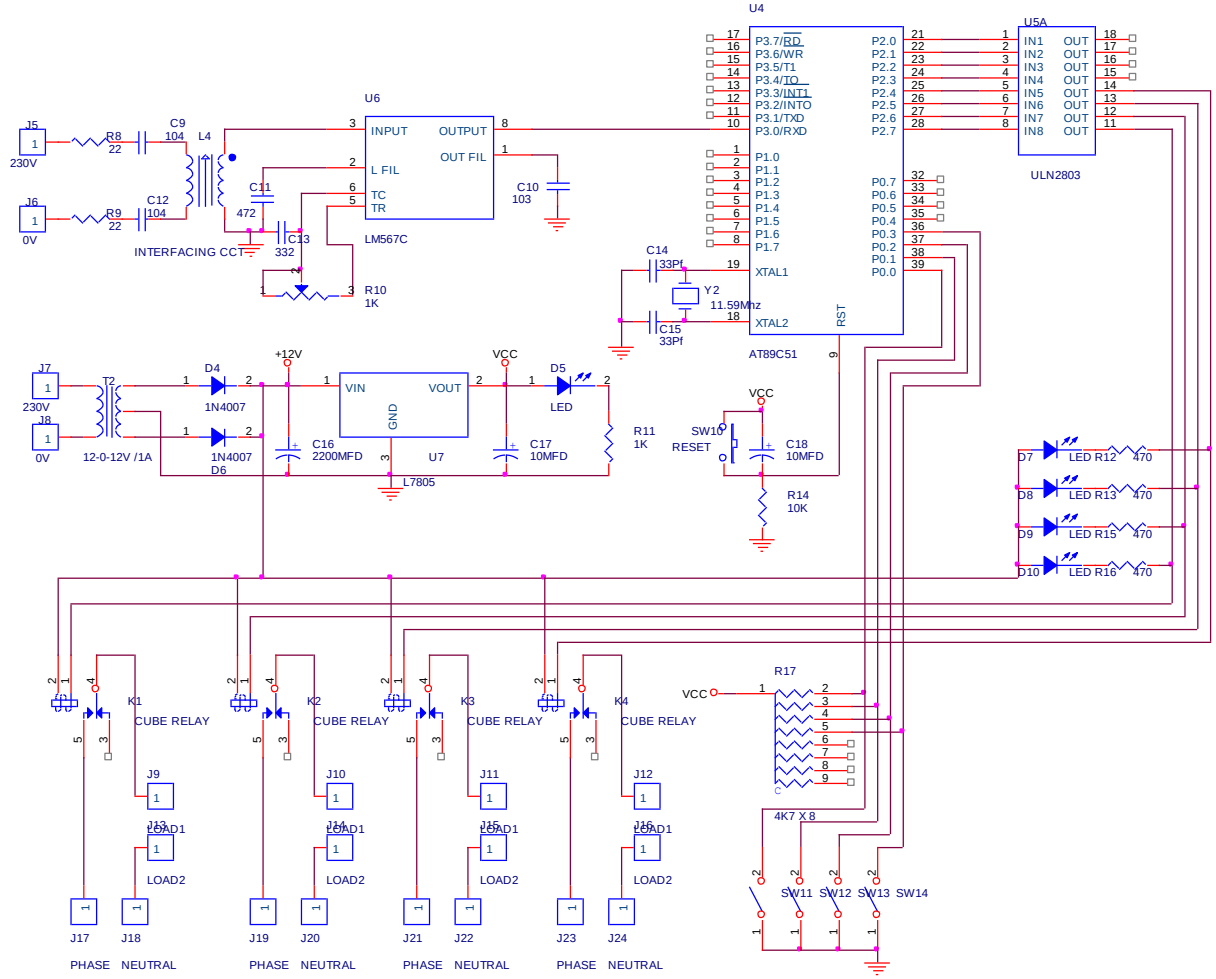


Fig5.2 Circuit diagram of Receiver section

Chapter 6
TESTING

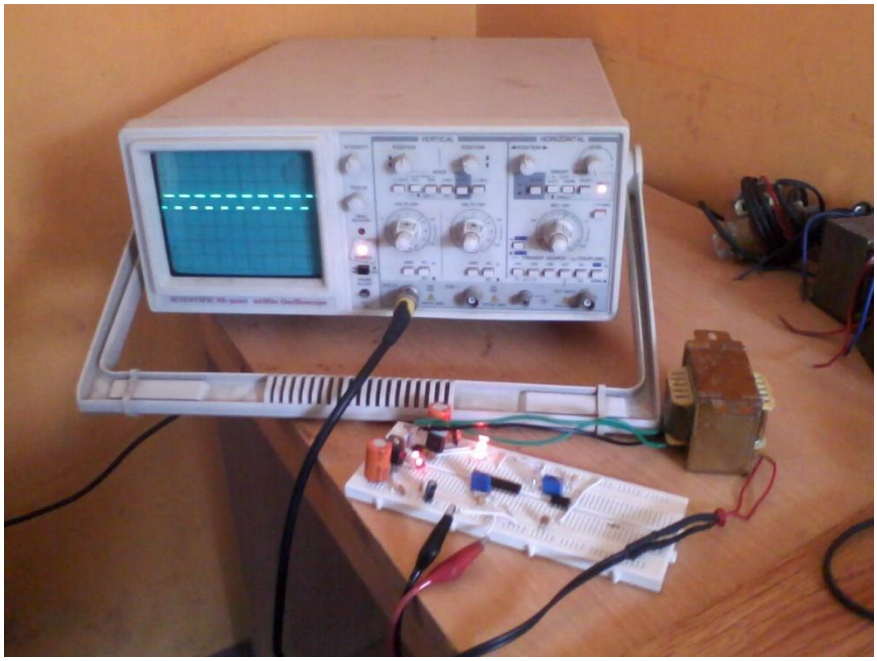


Fig6.1 Checking of output in CRO

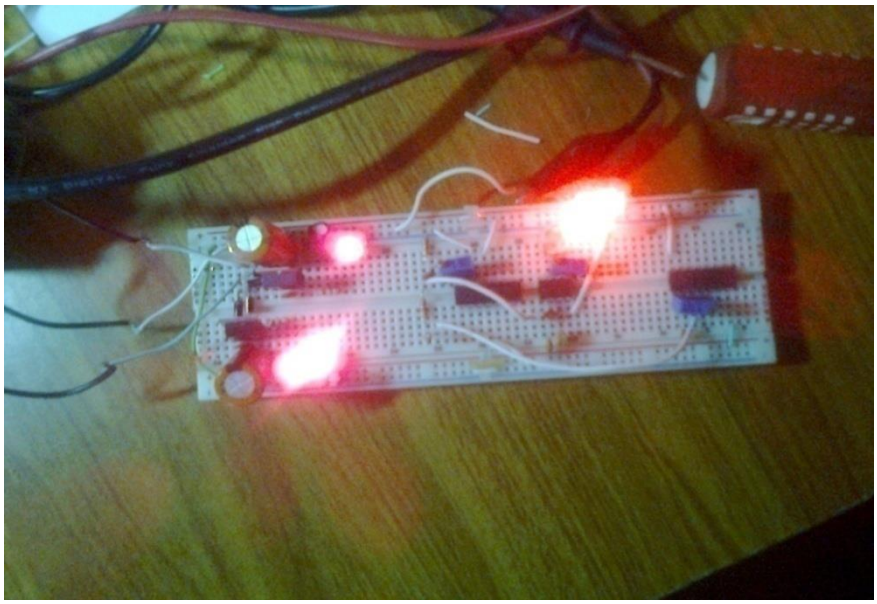


Fig6.2 Transmitter circuit on bread board

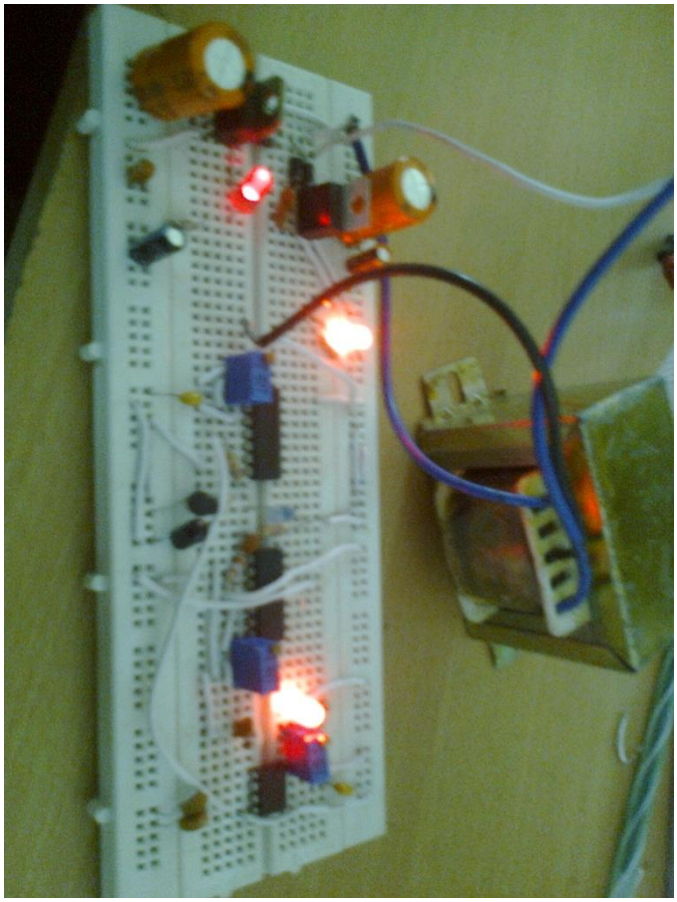


Fig6.3 Receiver circuit on bread board

Chapter 7
PCB DESIGN AND LAYOUT

The first step of assembling is to procure a printed circuit board. The fabrication of the program counter plays a crucial role in the electronic field. The success of a circuit is also depends on the PCB. As far as the cost is concerned the more than 25% of the total cost is gone for the PCB design and fabrication.

We are using a micro controller-based system that handles high frequencies. In the high frequency circuit the data may easily be violated in the PCB due to the physical parameters. That is the track capacitance and inductance can cause the cross talk in the buses. Also unwanted noise can be induced to supply rails and from there it can affect the total response. Hence the PCB design has a major role in the system performance.

Design of a PCB is consider as the last step in electronics circuit design as well as the first step in the production of the PCBs. It forms a distant factor in electronics circuit's performance and reliability. The productivity of the PCB and its assembly and service ability also depends on the design. The designing of the PCB consist of the designing of the layout followed by the generation of the artwork. Orcad is a low cost feature rich software package for designing electronics circuit diagrams. The various tools in Orcad and their implementation and designing the PCB are discussed below.

7.1 ELECTRONICS DESIGN AUTOMATION (EDA) TOOLS

With the advent of powerful computing system and interactive software, several stages in the design and development of an electronic circuit has undergone automation. The software and this hardware tool, which enable this automation, are called EDA tools. This tool helps us in such a way that we can draw that circuit; list the functioning of the circuit in response to the best inputs in assimilation software after successful simulating the circuit. The placing and routing software does the PCB artwork in the project the design automation tool used in Orcad, which includes.

7.1.1 ORCAD CAPTURE

For circuiting the circuit diagram, create schematic and net list.

7.1.2 ORCAD LAYOUT

For creating the PCB artwork the design process is of the following steps.

7.1.3 DRAWING THE CIRCUIT SCHEMATIC

This is done in Orcad schematic capture. It includes many libraries with thousands of component symbol. We can select the required symbol from library and place it on the schematic page. After placing the component symbol, the interconnection is completing using bus tool. After drawing the schematic, the following operations are performed.

7.1.4 ROUTING

Routing is the interconnection of component using upper tracks of required width. Before starting routing the following thinks are done.

7.1.5 ENABLING/DISABLING REQUIRED LAYERS

The number of layers used and enabling the artwork depends upon the complexity of the circuit, and fabrication technology available. If the board is single sided, enable only bottom or solder side layer, so that track will come only on one side of the PCB. If the circuit

is much more complex the enable the required number of inner layer consider the fabrication technique and cost.

7.1.6 MANUAL ROUTING

In this, the PCB design has to manually connect each track. This is time consuming process, but is required some cases. On this also the software checks for errors and reports.

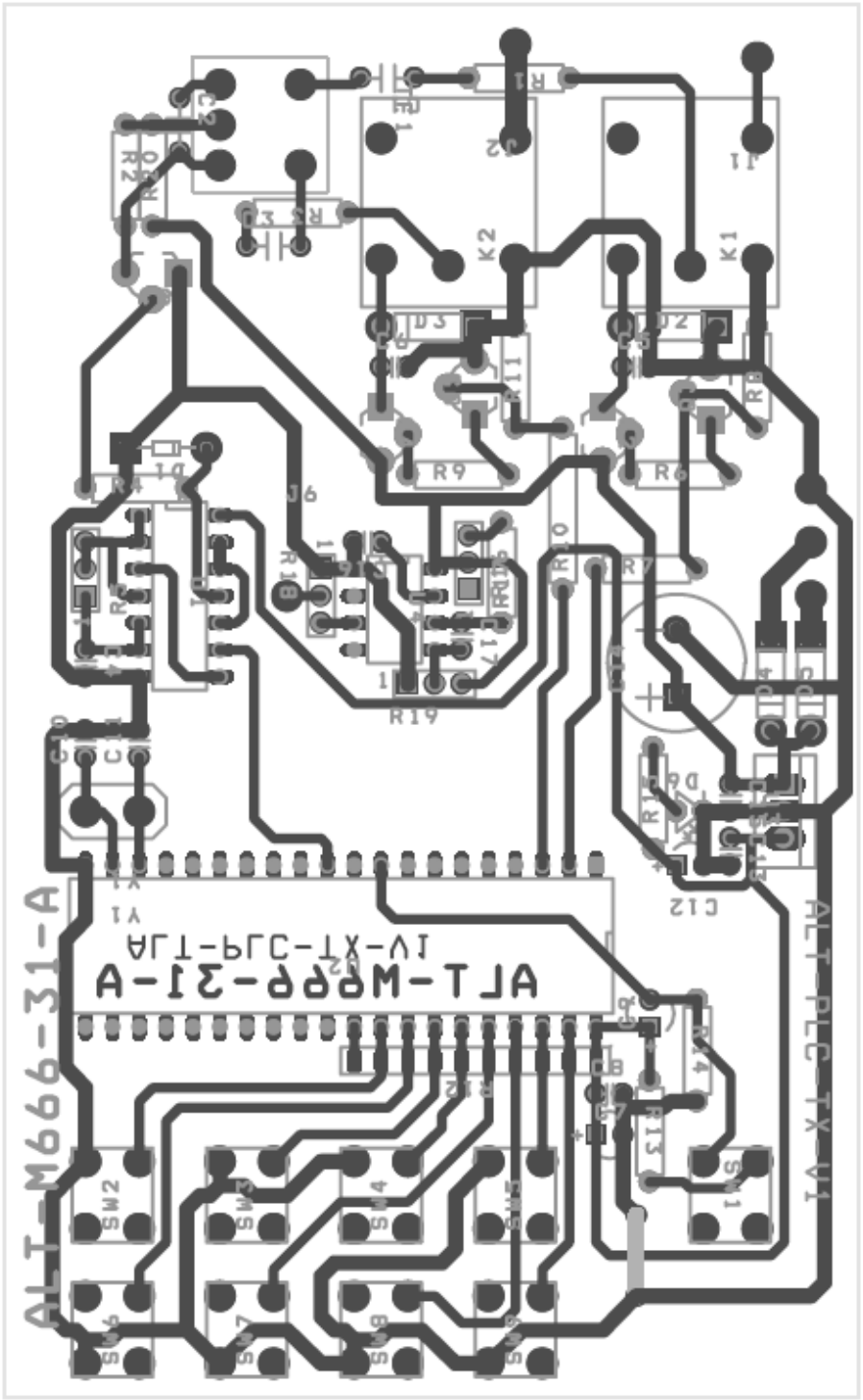


Fig7.1 Layout of Transmitter Circuit

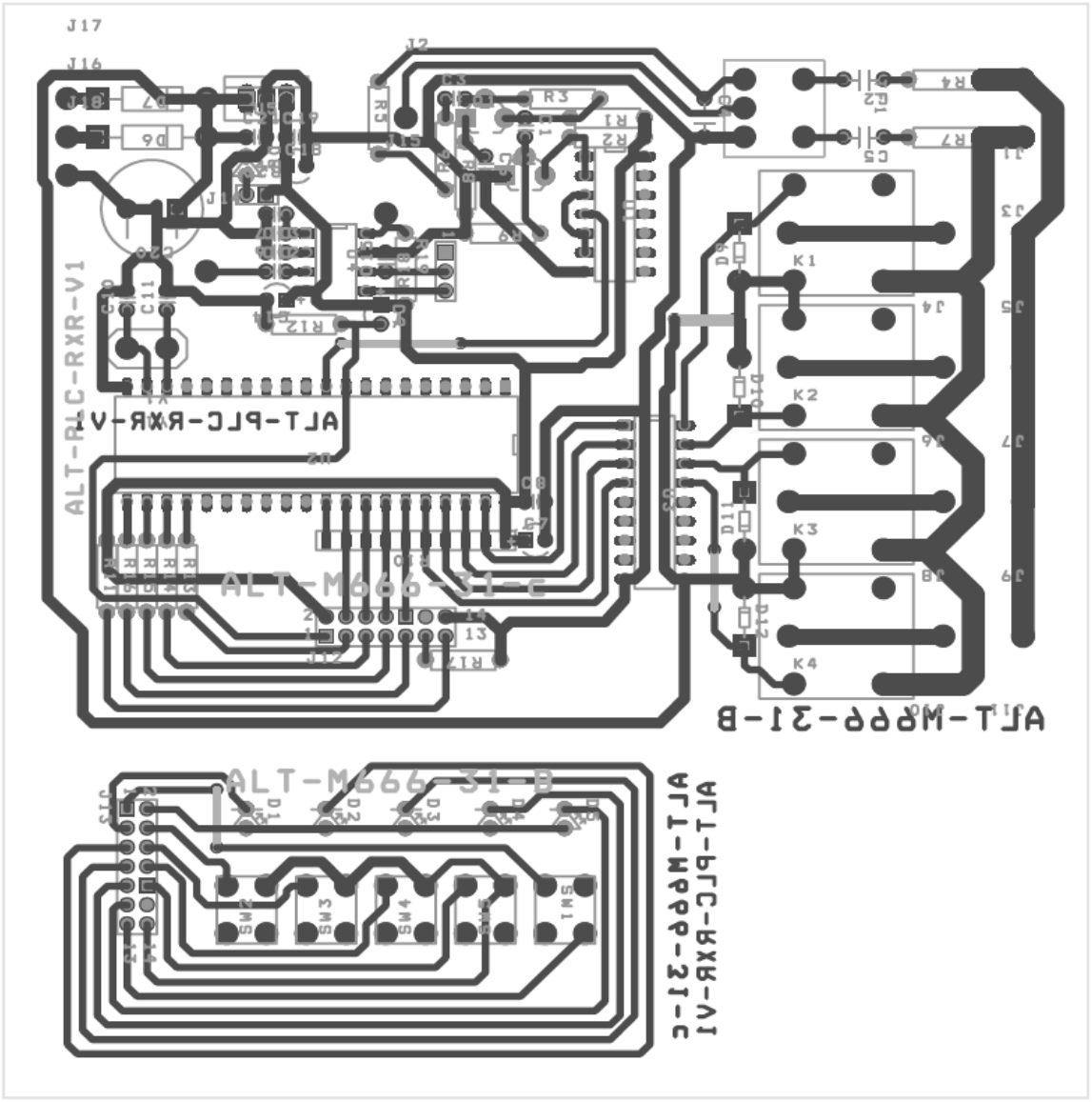


Fig7.2 Layout of Receiver Circuit

Chapter 8
SOFTWARE

8.1 PROGRAM FOR TRANSMITTER SECTION

```
SW1     EQU     P0.0
SW2     EQU     P0.1
SW3     EQU     P0.2
SW4     EQU     P0.3
SW5     EQU     P0.4
SW6     EQU     P0.5
SW7     EQU     P0.6
SW8     EQU     P0.7


        ORG     0000H

        MOV     SP,#50H         ; SP =50
        MOV     TMOD,#20H       ; TR0,TR1 IN AUTO RELOAD
        MOV     TH1,#E8H        ; TH1 = BAUD RATE, 6 A0 4 300
        SETB    TR1             ; TIMER RUNS AT 11059200/6*12*16 = 153600
        MOV     SCON,#40H       ; SCON = 0   1   0   0   0   0 0  0


START:  JNB     SW1,LOAD1
        JNB     SW1,LOAD2
        JNB     SW1,LOAD3
        JNB     SW1,LOAD4
        JNB     SW1,LOAD5
        JNB     SW1,LOAD6
        JNB     SW1,LOAD7
        JNB     SW1,LOAD8
        JNB     SW1,LOAD9
        JNB     SW1,LOAD10
        SJMP    START
;.....................................................................

LOAD1:  MOV     SBUF,#01H
SEND:   JNB     TI,SEND
        ACALL   DLY
        SJMP    START

;.....................................................................
```

```
LOAD2:    MOV     SBUF,#02H
          SJMP    SEND
;.....
LOAD3:    MOV     SBUF,#03H
          SJMP    SEND
;.....
LOAD4:    MOV     SBUF,#04H
          SJMP    SEND
;.....
LOAD5:    MOV     SBUF,#05H
          SJMP    SEND
;.....
LOAD6:    MOV     SBUF,#06H
          SJMP    SEND
;.....
LOAD7:    MOV     SBUF,#07H
          SJMP    SEND
;.....
LOAD8:    MOV     SBUF,#08H
          SJMP    SEND
;.....
LOAD9:    MOV     SBUF,#09H
          SJMP    SEND
;.....
LOAD10:   MOV     SBUF,#10H
          SJMP    SEND
;.....

                                ; delay subroutine for 0.5 Sec
DLY:      MOV     R0,#10        ; R0 =10
DL1:      MOV     R1,#200       ; R1=200
DL2:      MOV     R2,#250       ; R2=250
DL3:      DJNZ    R2,DL3        ; R2=R2-1 UP TO R2 =00, Delay for 250 µSec
          DJNZ    R1,DL2        ; t = 250 x 200 = 50000 µSec
          DJNZ    R0,DL1        ; t = 10x250x200 = 0.5 Sec
          RET                   ; RETURN
;.....
END
```

8.2 PROGRAM FOR RECEIVER SECTION

```
        SW1             EQU             P0.0
        SW2             EQU             P0.1
        SW3             EQU             P0.2
        SW4             EQU             P0.3
        SW5             EQU             P0.4

        RL1             EQU             P2.0
        RL2             EQU             P2.1
        RL3             EQU             P2.2
        RL4             EQU             P2.3
        RL5             EQU             P2.4

;.....................................................................

                ORG             0000H

                MOV             TMOD,#20H       ; TR0,TR1 IN AUTO RELOAD
                MOV             TH1,#E8H        ; TH1 = BAUD RATE, 6 A0 4 300
                SETB            TR1             ; TIMER RUNS AT 11059200/6*12*16 = 153600
                MOV             SCON,#50H       ; SCON = 0   1   0   1   0   0 0  0

;.....................................................................

START:          JB              RI,SWITCH       ; GOTO SWITCH IF ANY DATA RECEIVED
                JB              SW1,START1      ; GO TO START1 IS SWITCH OPEN
                CPL             RL1             ; COMPLIMENT RELAY1 IF SWITCH CLOSED
                SJMP            DLY

START1:         JB              SW2,START2      ; CHECK SWITCH 2
                CPL             RL2             ; COMPLIMENT RELAY2 IF SWITCH CLOSED
                SJMP            DLY

START2:         JB              SW3,START3      ; CHECK SWITCH 3
                CPL             RL3             ; COMPLIMENT RELAY3 IF SWITCH CLOSED
                SJMP            DLY

START3:         JB              SW4,START       ; CHECK SWITCH 4
                CPL             RL4             ; COMPLIMENT RELAY4 IF SWITCH CLOSED
                SJMP            DLY

;.....................................................................
                                                ; delay subroutine for 0.5 Sec
DLY:            MOV             R0,#10          ; R0 =10
```

```
DL1:    MOV     R1,#200         ; R1=200
DL2:    MOV     R2,#250         ; R2=250
DL3:    DJNZ    R2,DL3          ; R2=R2-1 UP TO R2 =00, Delay for 250 µSec
        DJNZ    R1,DL2          ; t = 250 x 200 = 50000 µSec
        DJNZ    R0,DL1          ; t = 10x250x200 = 0.5 Sec
        SJMP    START                   ; RETURN
;.....

SWITCH: MOV     A,SBUF          ; COPY RECEIVED DATA TO ACCUMULATOR

        CJNE    A,#01H,SWR1     ; CHECK WHETEHER THE RECEIVED DATA =1
        SETB    RL1                     ; SWITCH ON RELAY 1
        SJMP    START                   ; GO TO EXIT

WR1:    CJNE    A,#02H,SWR2
        SETB    RL2                     ; SWITCH ON RELAY 2
        SJMP    START                   ; GO TO EXIT

SWR2:   CJNE    A,#03H,SWR3
        SETB    RL3                     ; SWITCH ON RELAY 3
        SJMP    START                   ; GO TO EXIT

SWR3:   CJNE    A,#04H,SWR4
        SETB    RL4                     ; SWITCH ON RELAY 4
        SJMP    START                   ; GO TO EXIT

SWR4:   CJNE    A,#05H,SWR5
        CLR     RL1                     ; SWITCH OFF RELAY 1
        SJMP    START                   ; GO TO EXIT

SWR5:   CJNE    A,#06H,SWR6
        CLR     RL2                     ; SWITCH OFF RELAY 2
        SJMP    START                   ; GO TO EXIT

SWR6:   CJNE    A,#07H,SWR7
        CLR     RL3                     ; SWITCH OFF RELAY 3
        SJMP    START                   ; GO TO EXIT

SWR7:   CJNE    A,#08H, START
        CLR     RL5                     ; SWITCH OFF RELAY 4
        SJMP    START                   ; GO TO EXIT
;.....
END
```

Chapter 9
IMPLEMENTATION AND PERFORMANCE ANALYSIS

The power supply unit employed in both transmitter and receiver delivers required power to the circuits as soon as the 230V supply is applied to the input of the step down power transformer. The power O reset circuit fitted to the reset pin of the microcontrollers will reset them thereby clearing the program counter as 0000h. The microcontroller will start fetching the codes as soon as the reset pin voltage falls to logic low level.

The program in the transmitter unit's microcontroller will always watch the logic level of the ports to which the switches are connected. The logic level at these ports will be at logic high level as far as the switches are kept open. The port pin will be connected to GND whenever the switch connected to that pin is closed, thereby making the voltage at this pin as logic low level.

The microcontroller will determine the code for the closed switch and this code will be transferred to the serial buffer of the transmitter unit in the UART. The UART will be pre-initialized with 1200 bps baud rate and 8-bit, no parity, 1-stop bit mode. The program further returns to algorithm where it looks the status of the switch.

The transmitter unit in the UART will shift out the code written to its serial buffer. The output of the uart is connected to the modulator gate, which will generate carrier for logic high level input and no carrier for logic low level input.

The carrier is transmitted over the 230V line to the receiver unit. The Phase Locked Loop in the receiver unit will demodulate this carrier frequency and give logic high level to the input of the RxD pin of the uart in the receiver‘s microcontroller. The UART in the receiver unit will convert the serial data into parallel format and intimate the microcontroller by setting the RI pin.

The program in the receiver's microcontroller will also scan the switches connected to it. The program will toggle the status of the relay; whenever the program detects the switch corresponding to that relay is closed. The program will also check the status of the RI flag and is reads the received data from the serial buffer of the receiver section of the UART. The received data will be compared with the codes assigned to each of the relay and the relay will be switched ON / off according the received data. The process will be executed until the systems are switched off.

Chapter 10
CONCLUSION

As per indicated in application, the power line provides wide areas of communication through all the channels, with this power line provides mobility, flexibility & stability because of its small size & portable size, internet accessibility & ease of installation. Power line communication is not so powered because of less inventions due to that cost required to design transceiver at each station is very high. So, today's point of view the first challenge is to reduce the cost. So, in future we definitely proved that power line communication is the most efficient, powerful & cheapest media of communication.

Addressing the individual project goals, a number of conclusions can be made. After detailed studies, we have gained an in-depth knowledge of the issues faced with power line carrier communications. The PLC system we designed is a primary stage of a home networking system in which we tried to send a data from one computer to another which is installed in the same building. A successful power line carrier communication link could be created by the addition of frequency hopping, variable gain stage and error correction techniques.